**Problem Statement :- Implement Full Adder using Behavioral Modeling**

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-- Company:

-- Engineer:

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-- Create Date: 16:05:20 09/24/2015

-- Design Name:

-- Module Name: FA - Behavioral

-- Project Name:

-- Target Devices:

-- Tool versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating

---- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity FA is

Port ( a : in STD\_LOGIC;

b : in STD\_LOGIC;

c : in STD\_LOGIC;

sum : out STD\_LOGIC;

carry : out STD\_LOGIC);

end FA;

architecture Behavioral of FA is

begin

process(a,b,c)

begin

if(a='1' and b='1' and c='1') then sum <='1' ; carry <='1';

elsif (a='1' and b='1' and c='0') then sum <='0' ; carry <='1';

elsif(a='1' and b='0' and c='1') then sum <='0' ; carry <='1';

elsif(a='1' and b='0' and c='0') then sum <='1' ; carry <='0';

elsif(a='0' and b='1' and c='1') then sum <='0' ; carry <='1';

elsif(a='0' and b='1' and c='0') then sum <='1' ; carry <='0';

elsif(a='0' and b='0' and c='1') then sum <='1' ; carry <='0';

else

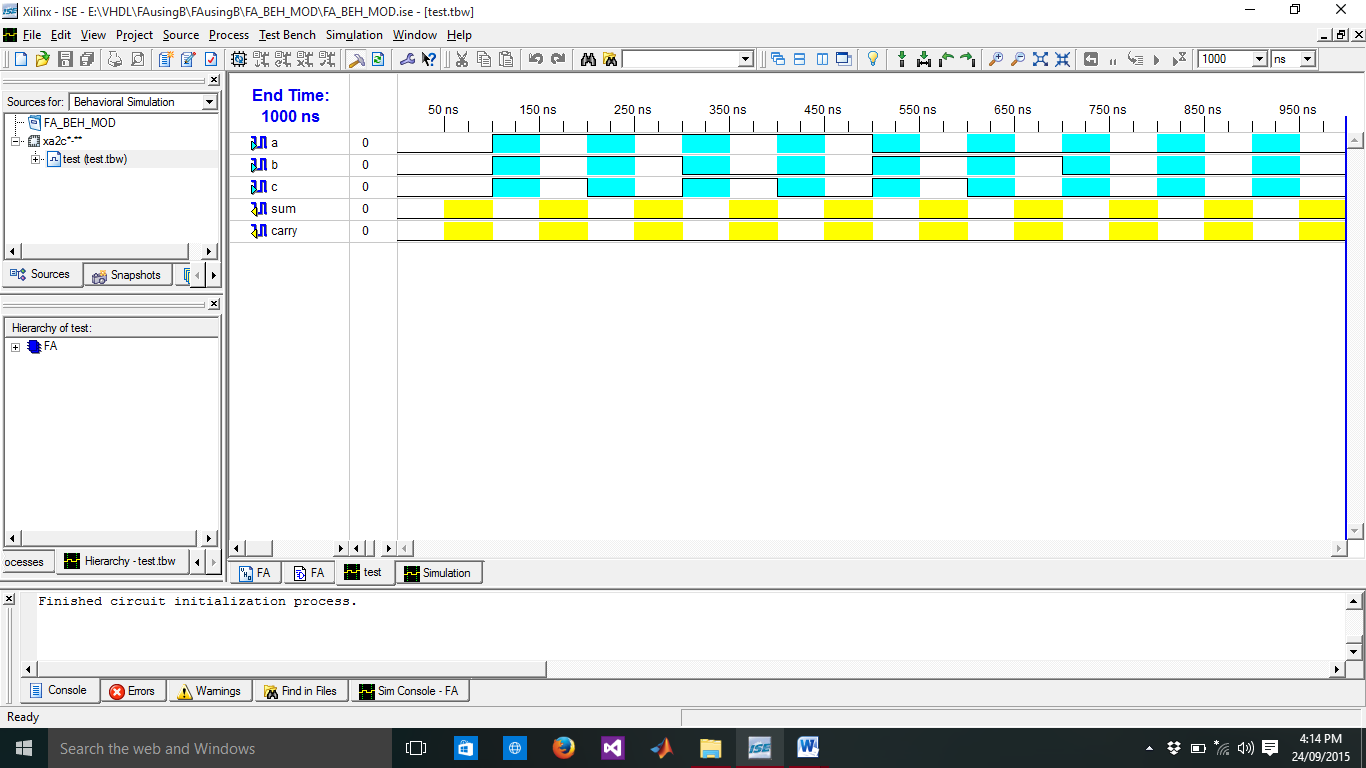
sum<='0'; carry<='0';

end if;

end process;

end Behavioral;

**Input Waveforms:**



**Output Waveforms:**

